Features

- Smallest footprint in chip-scale (CSP): 1.5 x 0.8 mm
- Fixed 32.768 kHz
- <10 ppm frequency tolerance
- Ultra-low power: <1 µA
- Directly interfaces to XTAL inputs
- Supports coin-cell or super-cap battery backup voltages
- Vdd supply range: 1.5V to 3.63V over -40°C to +85°C
- Oscillator output eliminates external load caps
- Internal filtering eliminates external Vdd bypass cap
- NanoDrive™ programmable output swing for lowest power

Applications

- Mobile Phones, Tablets, Health and Wellness Monitors, Fitness Watches
- Sport Video Cams, Wireless Keypads, Ultra-Small Notebook PC
- Pulse-per-Second (pps) Timekeeping, RTC Reference Clock

TempFlat MEMS™

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency and Stability						
Fixed Output Frequency	Fout		32.768		kHz	
Frequency Stability						
Frequency Tolerance [1]	F_tol			10	ppm	T_A = 25°C, post reflow, Vdd: 1.5V – 3.63V.
				20	ppm	T_A = 25°C, post reflow with board-level underfill, Vdd: 1.5V – 3.63V.
Frequency Stability [2]	F_stab			75	ppm	T_A = -10°C to +70°C, Vdd: 1.5V – 3.63V.
				100		T_A = -40°C to +85°C, Vdd: 1.5V – 3.63V.
				250		T_A = -10°C to +70°C, Vdd: 1.2V – 1.5V.
25°C Aging		-1		1	ppm	1st Year
Supply Voltage and Current Consumption						
Operating Supply Voltage	Vdd	1.2		3.63	V	T_A = -10°C to +70°C
		1.5		3.63	V	T_A = -40°C to +85°C
Core Operating Current [3]	Idd		0.90		µA	T_A = 25°C, Vdd: 1.8V. No load
				1.3		T_A = -10°C to +70°C, Vdd max: 3.63V. No load
				1.4		T_A = -40°C to +85°C, Vdd max: 3.63V. No load
Output Stage Operating Current [3]	Idd_out		0.065	0.125	µA/Vpp	T_A = -40°C to +85°C, Vdd: 1.5V – 3.63V. No load
Power-Supply Ramp	t_Vdd_Ramp			100	ms	Vdd Ramp-up from 0 to 90%, T_A = -40°C to +85°C
Start-up Time at Power-up [4]	t_start		180	300	ms	T_A = -40°C ≤ T_A ≤ +50°C, valid output
				450		T_A = +50°C < T_A ≤ +85°C, valid output
Operating Temperature Range						
Commercial Temperature	T_use	-10		70	°C	
Industrial Temperature		-40		85	°C	

Notes:

1. Measured peak-to-peak. Tested with Agilent 53132A frequency counter. Due to the low operating frequency, the gate time must be ≥100 ms to ensure an accurate frequency measurement.
2. Measured peak-to-peak. Inclusive of Initial Tolerance at 25°C, and variations over operating temperature, rated power supply voltage and load. Stability is specified for two operating voltage ranges. Stability progressively degrades with supply voltage below 1.5V.
3. Core operating current does not include output driver operating current or load current. To derive total operating current (no load), add core operating current + (0.065 µA/V) * (output voltage swing).
4. Measured from the time Vdd reaches 1.5V.

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32KHZ Ultra small Oscillators

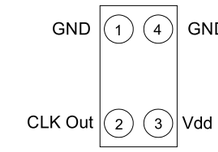
Electrical Characteristics (continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVCMOS Output Option, T_A = -40°C to +85°C, typical values are at T_A = 25°C						
Output Rise/Fall Time	tr, tf		100	200	ns	10-90% (Vdd), 15 pF load, Vdd = 1.5V to 3.63V
				50		10-90% (Vdd), 5 pF load, Vdd ≥ 1.62V
Output Clock Duty Cycle	DC	48		52	%	
Output Voltage High	VOH	90%			V	Vdd: 1.5V – 3.63V. I_{OH} = -10 µA, 15 pF
Output Voltage Low	VOL			10%	V	Vdd: 1.5V – 3.63V. I_{OL} = 10 µA, 15 pF
NanoDrive™ Programmable, Reduced Swing Output						
Output Rise/Fall Time	tf, tf			200	ns	30-70% (V_{OL}/V_{OH}), 10 pF Load
Output Clock Duty Cycle	DC	48		52	%	
AC-coupled Programmable Output Swing	V_sw		0.20 to 0.80		V	YSO1532MK does not internally AC-couple. This output description is intended for a receiver that is AC-coupled. See Table 2 for acceptable NanoDrive swing options.Vdd: 1.5V – 3.63V, 10 pF Load, I_{OH} / I_{OL} = ±0.2 µA. Vdd: 1.5V – 3.63V. I_{OH} = -0.2 µA, 10
DC-Biased Programmable Output Voltage High Range	VOH		0.60 to 1.225		V	pF Load. See Table 1 for acceptable V_{OH}/V_{OL} setting levels. Vdd: 1.5V – 3.63V. I_{OL} = 0.2 µA, 10 pF Load. See Table 1 for
DC-Biased Programmable Output Voltage Low Range	VOL		0.35 to 0.80		V	acceptable V_{OH}/V_{OL} setting levels.
Programmable Output Voltage Swing Tolerance		-0.055		0.055	V	T_A = -40°C to +85°C, Vdd = 1.5V to 3.63V.
Jitter						
Period Jitter	T_jitt		35		ns_{RMS}	Cycles = 10,000, T_A = 25°C, Vdd = 1.5V – 3.63V

Pin Configuration

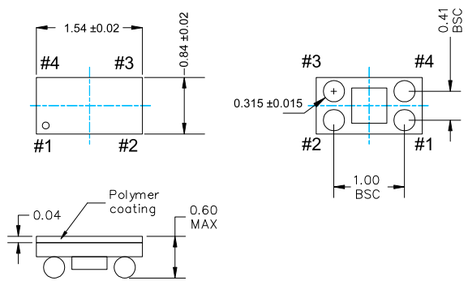
Pin	Symbol	I/O	Functionality
1, 4	GND	Power Supply Ground	Connect to ground. Acceptable to connect pin 1 and 4 together. Both pins must be connected to GND.
2	CLK Out	OUT	Oscillator clock output. The CLK can drive into a Ref CLK input or into an ASIC or chip-set's 32kHz XTAL input. When driving into an ASIC or chip-set oscillator input (X IN and X Out), the CLK Out is typically connected directly to the XTAL IN pin. No need for load capacitors. The output driver is intended to be insensitive to capacitive loading.
3	Vdd	Power Supply	Connect to power supply 1.2V ≤ Vdd ≤ 3.63V. Under normal operating conditions, Vdd does not require external bypass/decoupling capacitor(s). For more information about the internal power-supply filtering, see the *Power Supply Noise Immunity* section in the detailed description. Contact factory for applications that require a wider operating supply voltage range.

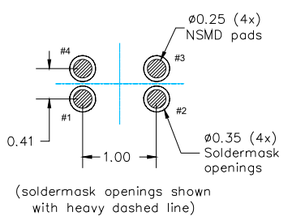
CSP Package (Top View)



Dimensions and Patterns

Package Size – Dimensions (Unit: mm)	Recommended Land Pattern (Unit: mm)
1.55 x 0.85 mm CSP	





Recommend 4-mil (0.1mm) stencil thickness

PART Number Guide

Quartz Crystal Oscillator	Dimensions	Frequency (Hz)	Frequency Stability Overall (ppm)	Output	Pin	Material	Operating Temp. Range
O	1508	32768K	S	D14	4	M	I

System Block Diagram

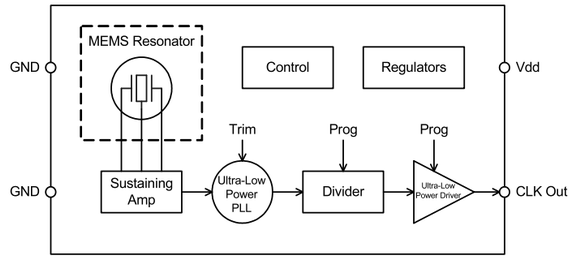


Figure 1.

Absolute Maximum

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Condition	Value	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 3.63	V
Short Duration Maximum Power Supply Voltage (Vdd)	<30 minutes	4.0	V
Continuous Maximum Operating Temperature Range	Vdd = 1.5V - 3.63V	105	°C
Short Duration Maximum Operating Temperature Range	Vdd = 1.5V - 3.63V, ≤30 mins	125	°C
Human Body Model ESD Protection	HBM, JESD22-A114	3000	V
Charge-Device Model (CDM) ESD Protection	JESD220C101	750	V
Machine Model (MM) ESD Protection	T_A = 25°C	300	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	Mil 883, Method 2002	10,000	g
Mechanical Vibration Resistance	Mil 883, Method 2007	70	g
1508 CSP Junction Temperature		150	°C

Features

- Small SMD package: 2.0 x 1.2 mm (2012)[1]
- Pin-compatible to 2012 XTAL SMD package
- Fixed 32.768 kHz output frequency
- <20 ppm frequency tolerance
- Ultra-low power: <1 µA
- Supports coin-cell or super-cap battery backup voltages
- Vdd supply range: 1.5V to 3.63V over -40°C to +85°C
- Oscillator output eliminates external load caps
- Internal filtering eliminates external Vdd bypass cap
- NanoDrive™ programmable output swing for lowest power

Applications

- Mobile Phones, Tablets, Health and Wellness Monitors, Fitness Watche
- Sport Video Cams, Wireless Keypads, Ultra-Small Notebook PC
- Pulse-per-Second (pps) Timekeeping, RTC Reference Clock

Note: 1. For the smallest 32 kHz XO in CSP (1.2mm^2), consider the YSO1532MK

TempFlat MEMS™

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency and Stability						
Fixed Output Frequency	Fout		32.768		kHz	
Frequency Stability						
Frequency Tolerance [2]	F_tol			20	ppm	T_A = 25°C, post reflow, Vdd: 1.5V – 3.63V.
Frequency Stability [3]	F_stab			75	ppm	T_A = -10°C to +70°C, Vdd: 1.5V – 3.63V.
				100		T_A = -40°C to +85°C, Vdd: 1.5V – 3.63V.
				250		T_A = -10°C to +70°C, Vdd: 1.2V – 1.5V.
25°C Aging		-1		1	ppm	1st Year
Supply Voltage and Current Consumption						
Operating Supply Voltage	Vdd	1.2		3.63	V	T_A = -10°C to +70°C
		1.5		3.63	V	T_A = -40°C to +85°C
Core Operating Current [4]	Idd		0.90		µA	T_A = 25°C, Vdd: 1.8V. No load
				1.3		T_A = -10°C to +70°C, Vdd max: 3.63V. No load
				1.4		T_A = -40°C to +85°C, Vdd max: 3.63V. No load
Output Stage Operating Current [4]	Idd_out		0.065	0.125	µA/Vpp	T_A = -40°C to +85°C, Vdd: 1.5V – 3.63V. No load
Power-Supply Ramp	t_Vdd_Ramp			100	ms	T_A = -40°C to +85°C, 0 to 90% Vdd
Start-up Time at Power-up [5]	t_start		180	300	ms	T_A = -40°C ≤ T_A ≤ +50°C, valid output
				450		T_A = +50°C < T_A ≤ +85°C, valid output
Operating Temperature Range						
Commercial Temperature	T_use	-10		70	°C	
Industrial Temperature		-40		85	°C	

Notes:

2. Measured peak-to-peak. Tested with Agilent 53132A frequency counter. Due to the low operating frequency, the gate time must be ≥100 ms to ensure an accurate frequency measurement.
3. Stability is specified for two operating voltage ranges. Stability progressively degrades with supply voltage below 1.5V. Measured peak-to-peak. Inclusive of Initial Tolerance at 25°C, and variations over operating temperature, rated power supply voltage and load.
4. Core operating current does not include output driver operating current or load current. To derive total operating current (no load), add core operating current + (0.065 µA/V) * (peak-to-peak output Voltage swing).
5. Measured from the time Vdd reaches 1.5V.

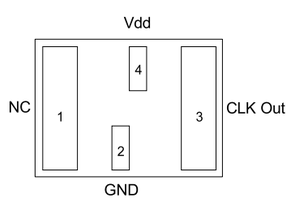
Electrical Characteristics (continued)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
LVCMOS Output Option, T_A = -40°C to +85°C, typical values are at T_A = 25°C						
Output Rise/Fall Time	tr, tf		100	200	ns	10-90% (Vdd), 15 pF load, Vdd = 1.5V to 3.63V
				50		10-90% (Vdd), 5 pF load, Vdd ≥ 1.62V
Output Clock Duty Cycle	DC	48		52	%	
Output Voltage High	VOH	90%			V	Vdd: 1.5V – 3.63V. I_{OH} = -10 µA, 15 pF
Output Voltage Low	VOL			10%	V	Vdd: 1.5V – 3.63V. I_{OL} = 10 µA, 15 pF
NanoDrive™ Programmable, Reduced Swing Output						
Output Rise/Fall Time	tf, tf			200	ns	30-70% (V_{OL}/V_{OH}), 10 pF Load
Output Clock Duty Cycle	DC	48		52	%	
AC-coupled Programmable Output Swing	V_sw		0.20 to 0.80		V	YSO1533MK does not internally AG-couple. This output description is intended for a receiver that is AC-coupled. See Table 2 for acceptable NanoDrive swing options. Vdd: 1.5V – 3.63V, 10 pF Load, I_{OH} / I_{OL} = ±0.2 µA.
DC-Biased Programmable Output Voltage High Range	VOH		0.60 to 1.225		V	Vdd: 1.5V – 3.63V. I_{OH} = -0.2 µA, 10 pF Load. See Table 1 for acceptable V_{OH}/V_{OL} setting levels.
DC-Biased Programmable Output Voltage Low Range	VOL		0.35 to 0.80		V	Vdd: 1.5V – 3.63V. I_{OL} = 0.2 µA, 10 pF Load. See Table 1 for acceptable V_{OH}/V_{OL} setting levels.
Programmable Output Voltage Swing Tolerance		-0.055		0.055	V	T_A = -40°C to +85°C, Vdd = 1.5V to 3.63V.
Period Jitter	T_jitt		35		ns_{RMS}	Cycles = 10,000, T_A = 25°C, Vdd = 1.5V – 3.63V

Pin Configuration

SMD Pin	Symbol	I/O	Functionality
1	NC	No Connect	No Connect. Will not respond to any input signal. When interfacing to an MCU's XTAL input pins, this pin is typically connected to the receiving IC's X Out pin. In this case, the YSO1533MK will not be affected by the signal on this pin. If not interfacing to an XTAL oscillator, leave pin1 floating (no connect).
2	GND	Power Supply Ground	Connect to ground. All GND pins must be connected to power supply ground.
3	CLK Out	OUT	Oscillator clock output. When interfacing to an MCU's XTAL, the CLK Out is typically connected to the receiving IC's X IN pin. The YSO1533MK oscillator output includes an internal driver. As a result, the output swing and operation is not dependent on capacitive loading.This makes the output much more flexible, layout independent, and robust under changing environmental and manufacturing conditions.
4	Vdd	Power Supply	Connect to power supply 1.5V ≤ Vdd≤ 3.63V for operation over -40°C to +85°C temperature range. Under normal operatingconditions, Vdd does not require external bypass/decoupling capacitor(s). Internal powersupply filtering will reject more than ±150 mVpp with frequency components through 10MHz.Contact factory for applications that require a wider operating supply voltage range.

SMD Package (Top View)



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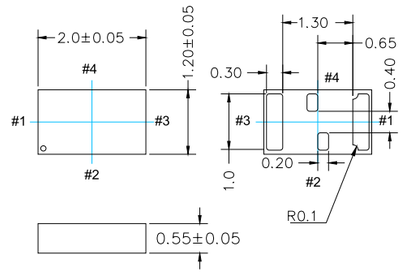
Dimensions and Patterns

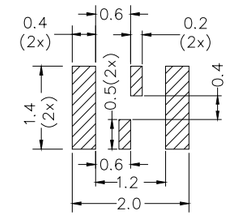
Package Size – Dimensions (Unit: mm)

2.0 x 1.2 mm SMD

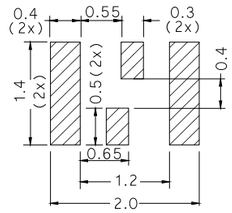


Recommended Land Pattern (Unit: mm)

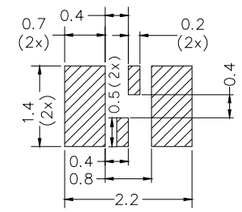
YXC Only SPL



YXC Alternate SPL with Larger Center Pads



XTAL Compatible SPL



PART Number Guide

Quartz Crystal Oscillator	Dimensions	Frequency (Hz)	Frequency Stability Overall (ppm)	Output	Pin	Material	Operating Temp. Range
O	2012	32768K	S	D14	4	M	I

System Block Diagram

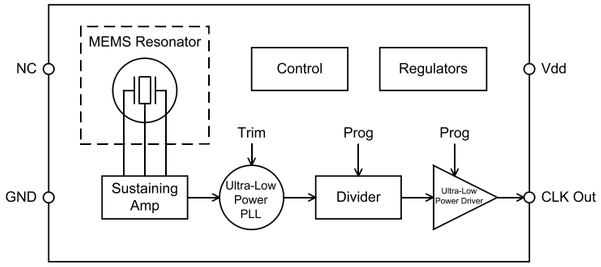
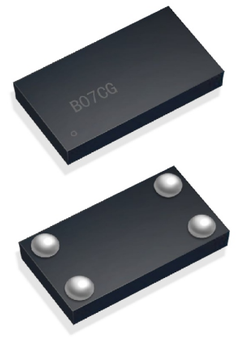


Figure 1.

Absolute Maximum

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Condition	Value	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 3.63	V
Short Duration Maximum Power Supply Voltage (Vdd)	≤30 minutes, over -40°C to +85°C	4.0	V
Continuous Maximum Operating Temperature Range	Vdd = 1.5V - 3.63V	105	°C
Short Duration Maximum Operating Temperature Range	Vdd = 1.5V - 3.63V, ≤30 mins	125	°C
Human Body Model ESD Protection	HBM, JESD22-A114	3000	V
Charge-Device Model (CDM) ESD Protection	JESD220C101	750	V
Machine Model (MM) ESD Protection	T_A = 25°C	300	V
Latch-up Tolerance	JESD78 Compliant		
Mechanical Shock Resistance	Mil 883, Method 2002	10,000	g
Mechanical Vibration Resistance	Mil 883, Method 2007	70	g
2012 SMD Junction Temperature		150	°C
Storage Temperature		-65°C to 150°C	



Features

- 32.768 kHz ±5, ±10, ±20 ppm frequency stability options over temp
- World’s smallest TCXO in a 1.5 x 0.8 mm CSP
- Operating temperature ranges: 0°C to +70°C ， -40°C to +85°C
- Ultra-low power: <1 µA
- Vdd supply range: 1.5V to 3.63V
- Improved stability reduces system power with fewer network timekeeping updates
- NanoDrive™ programmable output swing for lowest power and direct XTAL SoC input interface
- Internal filtering eliminates external Vdd bypass cap and saves space

Applications

- Smart Meters (AMR), Health and Wellness Monitors
- Pulse-per-Second (pps) Timekeeping, RTC Reference Clock

TempFlat MEMS™

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency and Stability						
Output Frequency	Fout		32.768		kHz	
Frequency Stability Over Temperature [1] (without Initial Offset [2])	F_stab	-5.0		5.0	ppm	
		-10		10		
		-20		20		
Frequency Stability Over Temperature (with Initial Offset [2])	F_stab	-10		10	ppm	
		-13		13		
		-22		22		
Frequency Stability vs Voltage	F_vdd	-0.75		0.75	ppm	1.8V ±10%
		-1.5		1.5	ppm	1.5V – 3.63V
First Year Frequency Aging	F_aging	-1.0		1.0	ppm	T_A = 25°C, Vdd = 3.3V
Jitter Performance (T_A = over temp)						
Long Term Jitter				2.5	ps_{pp}	81920 cycles (2.5 sec), 100 samples
Period Jitter			35		ns_{RMS}	Cycles = 10,000, T_A = 25°C, Vdd = 1.5V – 3.63V
Supply Voltage and Current Consumption						
Operating Supply Voltage	Vdd	1.5		3.63	V	T_A = -40°C to +85°C
Core Supply Current [3]	Idd		0.99		µA	T_A = 25°C, Vdd = 1.8V, LVCMOS Output configuration, No Load
				1.52		T_A = -40°C to +85°C, Vdd = 1.5V – 3.63V, No Load
Power-Supply Ramp	t_Vdd_Ramp			100	ms	Vdd Ramp-Up 0 to 90% Vdd, T_A = -40°C to +85°C
Start-up Time at Power-up	t_start		180	300	ms	T_A = -40°C +60°C, valid output
				350		T_A = +60°C to +70°C, valid output
				380		T_A = +70°C to +85°C, valid output

Notes:

1. No board level underfill. Measured as peak-to-peak/2. Inclusive of 3x-reflow and ±20% load variation. Tested with Agilent 53132A frequency counter. Due to the low operating frequency, the gate time must be ≥100 ms to ensure an accurate frequency measurement.
2. Initial offset is defined as the frequency deviation from the ideal 32.768 kHz at room temperature, post reflow.
3. Core operating current does not include output driver operating current or load current. To derive total operating current (no load), add core operating current + output driver operating current, which is a function of the output voltage swing. See the description titled, **Calculating Load Current.**